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(54) Title of the invention Probe card

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Description

1. Title of invention

Inspection apparatus

2. Claim

An inspection apparatus comprising, a specimen stand to support a test substance, parallelism detecting means to detect a parallelism between the test substance and a probe needles array card, a parallelism control part to move said test substance and probe needles array card relatively to make them parallel each other based on the result from said parallelism detecting means, and inspecting means to inspect said test substance after the parallelism is controlled by said parallelism controlling unit.

3. Detailed description of the invention

[Field of invention]

The present invention relates to an inspection apparatus.

[Background of the invention]

When fine circuits formed in chips, which are constituents of silicon wafers, are inspected in order to check whether it is configured as the design specification, a circuit tester composed of a signal generator, and a waveform analyzer. In this case, a needle point of a needle of the probing card (trade name) is brought into pressure contact with a pad at a chip, and a test signal is applied from said circuit tester to said fine circuit through said needle point and pad to judge the pass-fail of the formation of said circuit in chip.

Meanwhile, the size of chip has been getting larger accompanied with the progress of recent very-large-scale-integration (VLSI) of semiconductors, for example, as shown in Figure 3, a large rectangular chip (51) whose size is equal to 3 consecutive conventional chips is formed on the silicon wafer (W). Large number of pads (52) for connecting with bond wires (not shown in Figures) are formed on the chip (51), as shown in Figure 4. When the pass-fail of said chip is inspected, as shown in Figure 5, the needle point of the needle (55) of the probing card (54) is brought into pressure contact with the surface to be tested of the pad (52) of chip (51) placed on a specimen stand (53) having a flat upper surface, and the circuit configuration is inspected whether it is conforming to the design specification by applying a test signal to the chip (51) from the circuit tester, which is not shown in Figures. Additionally, as can be clearly seen in Figure 4, each pad (52) is in pressure contact with each needle point of probe needle (55).

[Subjects to be solved by the invention]

However, for example in such a case as shown in

Figure 6, if the chip (51) and the needle point of the probing card (54) are not paralleled, the balance of pressure contact forces to pad (52) by the left needle and by the right one is not consistent. If the test signal is applied from said circuit tester under this inconsistent condition, since homogeneous signal application is not attained, there would be a possibility of misjudgment of pass-fail of the circuit formation.

The present invention was invented to solve said subjects, and the objective is to provide an inspection apparatus which can make the chip (specimen) and the probing card parallel.

[Methods to solve the subject]

To solve the subject, this invention is configured to comprise a specimen stand to support a test substance, parallelism detecting means to detect a parallelism between the test substance and a probe needles array card, a parallelism control part to move said test substance and probe needles array card relatively to make them parallel each other based on the result from said parallelism detecting means, and inspecting means to inspect said test substance after the parallelism is controlled by said parallelism controlling unit.

[Action of the invention]

According to the present invention, first, a trace is formed on the surface to be inspected of a specimen placed on a specimen stand by a pressure contact of a needle point of the probing card. And this trace is read by a trace reading part, which is a parallelism detecting means. In this case, if needle points have contact with surfaces to be tested under a condition that each needle is parallel to each surface, each size of trace should be approximately same, and if not, for example, the size of left trace should differ from that of the right one. More specifically, the surface to be inspected should be slanted against the probing card. Based on size of traces, the inclination judging part judges the inclinations of the probing card and test surface, and based on this judgment, the parallelism control part computes a calculation to make the probing card and the test surface parallel, and control the probing card and the test surface parallel to be parallel based on the calculation. When a test signal is applied from the circuit tester under a condition that the probing card and the test surface is parallel, accurate signals are applied to the test surface from each needle point of needle.

[Embodiment of the invention]

The embodiment of the present invention shall be described by referring Figure 1 and 2.

Meanwhile, the same symbol is added to the part which was already explained in Figure 3 to 5, and the duplicated explanation shall be omitted.

Figure 1 (A) is a block diagram to explain the embodiment of inspection apparatus for semiconductors.

As shown in Figure 1 (A), a test product such as a silicon wafer (W) is placed on the specimen stand (1), a supporting stand, which can move toward X, Y, Z and θ directions, and a plurality of square-shaped chips (51) are formed in the silicon wafer (W) (refer to Figure 3). The specimen stand (1) is placed on the pedestal (4), and as shown in Figure 1 (B), three servo motors (3a to 3c) are located at the apexes of an equilateral triangle in the pedestal (4). The placing surface (1a) of the specimen stand (1) can be inclined and adjusted toward all the direction, by the rotating driving of output axes (3d to 3f). Above the silicon wafer (W), the probing card (54) which is a probe driven by a vertical driving means (not shown in Figure) is placed. The probing card (54) is configured so that its needle points, wherein the electrode pattern needle points corresponding to said chip (51) are disposed, can be pressed and brought in contact with each pad (52) of the chip (51) of the silicon wafer (W), by the vertical movement of the silicon wafer (W). This probing card (54) is, for example, lifted upward from the position shown in Figure, and evacuated to right after the completion of said pressure contact. A trace readout part (5), which is a means to detect the parallelism and consisting of an imaging device such as CCD camera, is placed above the silicon wafer (W), and it reads out traces formed on the pad, based on the reflection of the light generated by the lamp (11) on the pad (52).

The CPU (6) is consisted of the inclination judging part (6a) and the parallelism control part (6b), and data (a pattern) read by the trace readout part (5) is converted to electric signal and sent to the inclination judging part (6a). The control signal is outputted so that the pattern information at several predetermined points become similar. By this output signal corresponding to the inclination data judged by said inclination judging part (6a), the parallelism control part (6b) drives said motors via motor driving parts (7a to 7c) to adjust the parallelism of the specimen stand (1), i.e., the parallelism of the wafer (W) surface. The ROM (8) installed with a program to control the entire inspection apparatus, and the RAM (9), which temporarily stores processed data, are connected to the CPU (6). Since the configuration of the semiconductor inspection apparatus is well known to those skilled in the art, the explanation is omitted.

Next, the action of the present invention shall be explained.

In a condition wherein the silicon wafer (W) is placed on the predetermined position of the specimen stand, the probe card (54) is driven to the predetermined position below by the vertical driving means, which is not shown in Figure, and the specimen table is moved upward and overdrive, then needle points of needles (55) are brought into pressure contact with pads (52). Now, it is assumed that large and small traces as shown in Figure 2 are formed on pads of selected chip in the wafer (W) by said pressure contact. More specifically, large traces (A_1 to A_4)are formed on left pads (52a, 52g, 52h and 52i), and the size of trace becomes smaller in inverse proportion to the increase of the distance between the pad, in which the trace is, and the left end of the chip, like B_1 to F_1, and B_4 to F_4. The nonparallelism between the probing card (54) and the chip (51) is judged based on these traces. More specifically, as shown in Figure 6, the distance between the probing card (54) and the chip (51) is shorter in left side, and longer in the right side. These are judged by using a pattern recognition technology. The condition described above is read out, in terms of the reflection of light emitted from the lamp (11) on the pad (52), by the trace read out part (5), as trace data. Said read out data is sent to the parallelism judging part (6a), and said parallelism judging part (6a) judges that the probing card (54) and the chip (51) are inclined each other based on the trace data. The parallelism control part (6b) computes a calculation to make the probing card (54) and the chip (51) parallel to each other based on the judgment data, and a movement, for example, an adjustment of the parallelism of the wafer (W) is performed. The results of the calculation are sent as parallelism control signals to each servo motor (3a to 3c) via each motor driving part (7a to 7c). Servo motors (3a to 3c) are rotated forward and reverse respectively corresponding to parallelism control signals (Ha to Hc), and the inclination of the specimen stand is controlled to adjust the probing card (54) and the chip (51) parallel to each other. Under this parallel condition, the predetermined test signal is applied from a circuit tester, which is not shown in Figure, and the judgment whether the circuit configuration of the chip is formed in conformance with the design specification.

In addition, the trace on the pad formed by the needlepoint of the probing card is used as a means to detect the parallelism in this embodiment, however instead of it, for example, ultrasonic sensors may be installed in the left and right sides of the specimen stand, and the distance between the specimen stand and the silicon wafer may be measured by emitting ultrasonic waves to a silicon wafer and reflecting on it, then predetermined calculation may be performed to decide the parallelism.

[Effect of the invention]

According to the present invention, for example, the degree of inclination of the needle point of the probing card to the chip is judged based on the size of a trace which is formed by a pressure contact of a needle point of the probing card, and the needle of the probing card and chip are adjusted to be parallel to each other, therefore an accurate test signal can be applied from the needle point of the probing card to the pad of the chip.

4. Brief description of drawings.

Figure 1 (A) and (B) are a block diagram and a plane view of the embodiment according to the present invention, respectively,

Figure 2 is a plane view showing the large and small traces,

Figure 3 is a plane view showing a silicon wafer, and a large chip,

Figure 4 is an enlarged view of the large chip,

Figure 5 is a view showing a condition wherein the needle point of the probe card is in pressure contact with a conventional large chip, and

Figure 6 is a side view showing an inappropriate contact between a conventional large chip and the probing card

Description of symbols

(1) specimen stand
(3a) to (3c) servo motor
(5) trace read out part
(6a) inclination judging part
(6b) parallel control unit]
(51) chip of a silicon wafer (specimen)
(54) probing card
(55) needle of the probing card
(A) to (F) trace
(W) silicon wafer

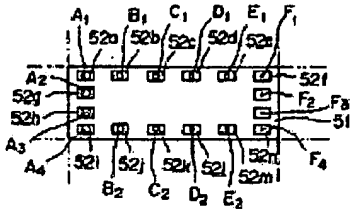

Figure 2

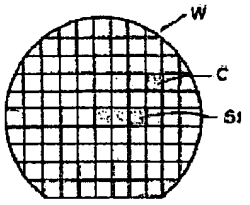

Figure 3

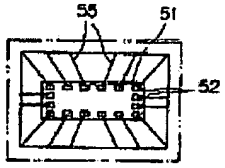

Figure 4

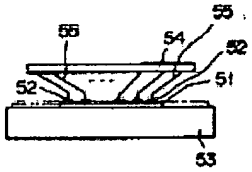

Figure 5

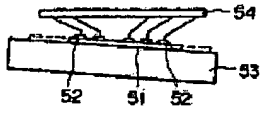

Figure 6

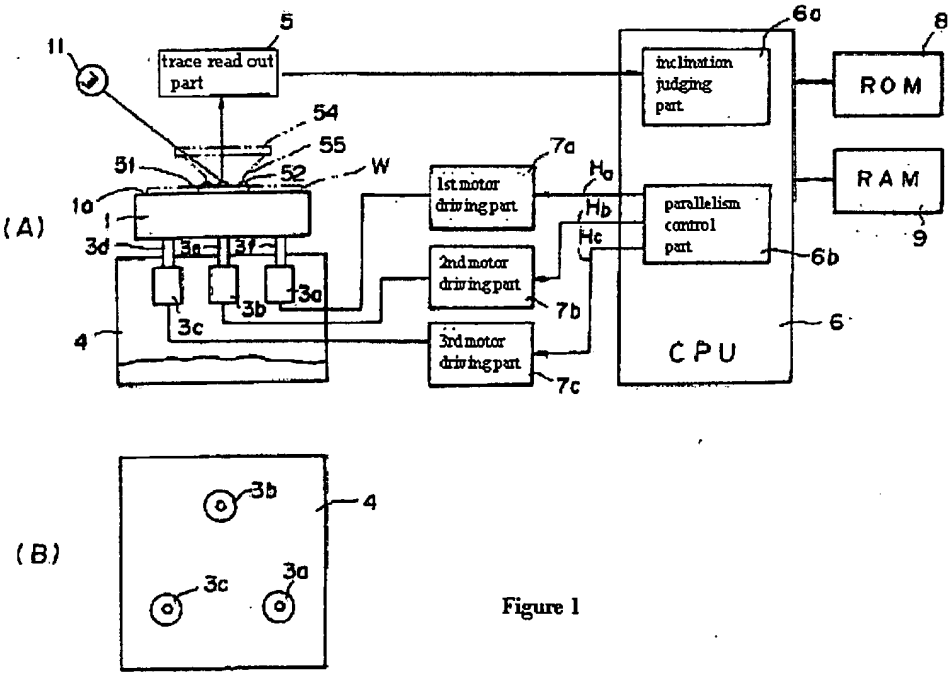

Figure 1

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CERTIFICATE OF TRANSLATION

April 2, 2007

I, Kagari Fujita, hereby certify that I am competent in both English and Japanese languages.

I further certify that under penalty of perjury translation of the aforementioned patent document:

[JP4207047A.pdf]

from the Japanese language into the English language is accurate and correct to the best of my knowledge and proficiency.

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